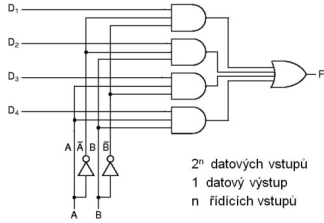


Multiplexer

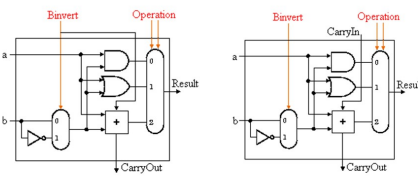


2ⁿ datových vstupů
1 datový výstup
n řídicích vstupů

ZS 2011

UPA

Jednabitová ALU



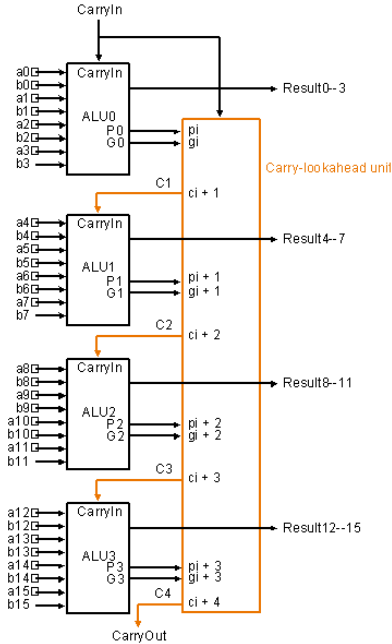
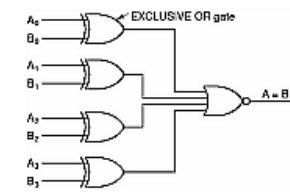
Bit s nejnižší vahou

Ostatní bity

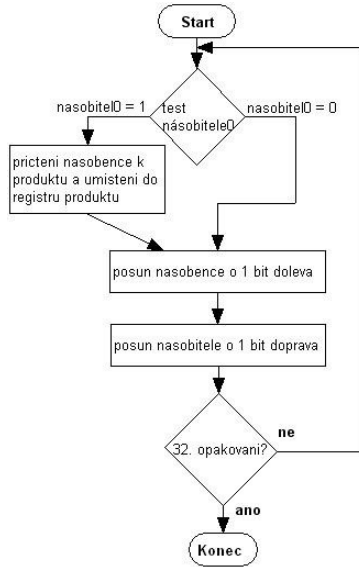
ZS 2011

UPA

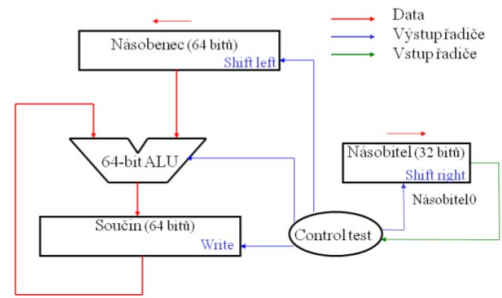
logický komparátor



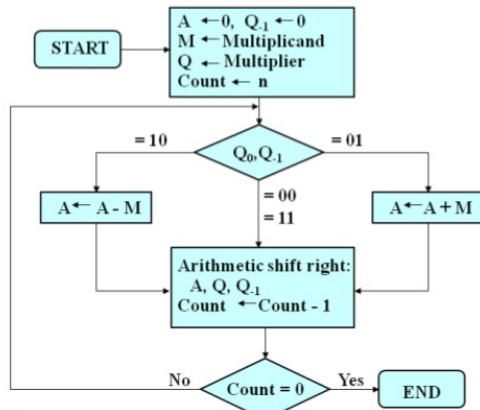
Operace násobení binárních čísel



Hardware (V.1)



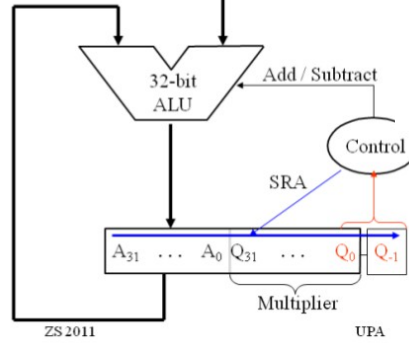
Boothův algoritmus



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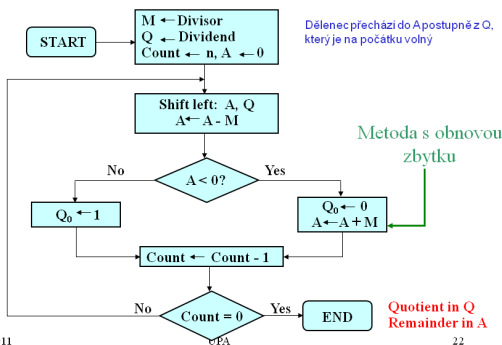
Typic algoritmus násob



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UPA

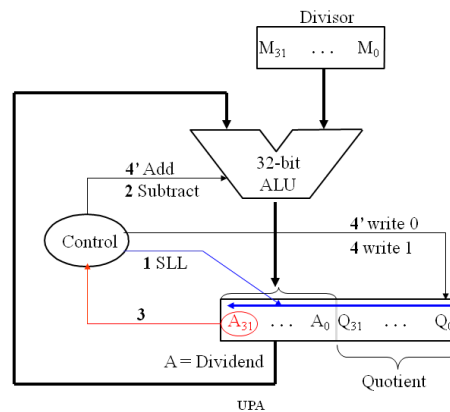
Dělení bez znaménka



ZS 2011

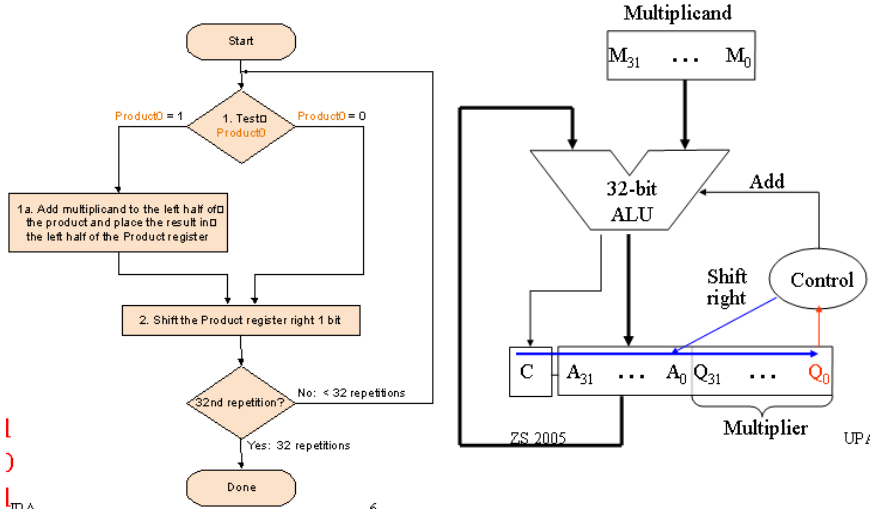
UPA

22

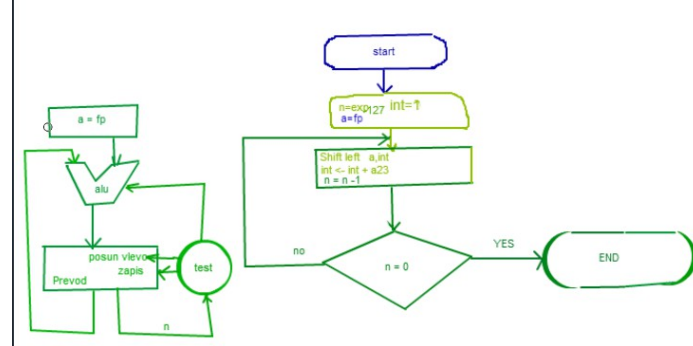


UPA

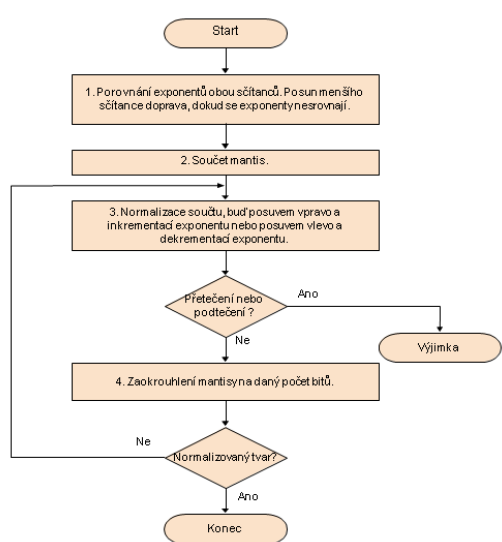
nasobeni kladnych cisel



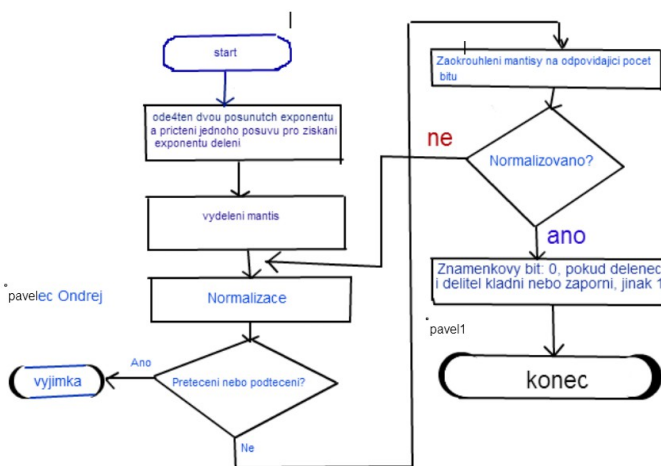
převod čísla float na int



sčítání dvou float



dělení float



násobení dvou float

